I2C & SPI

Master Synchronous Serial Port

ECE Senior Design

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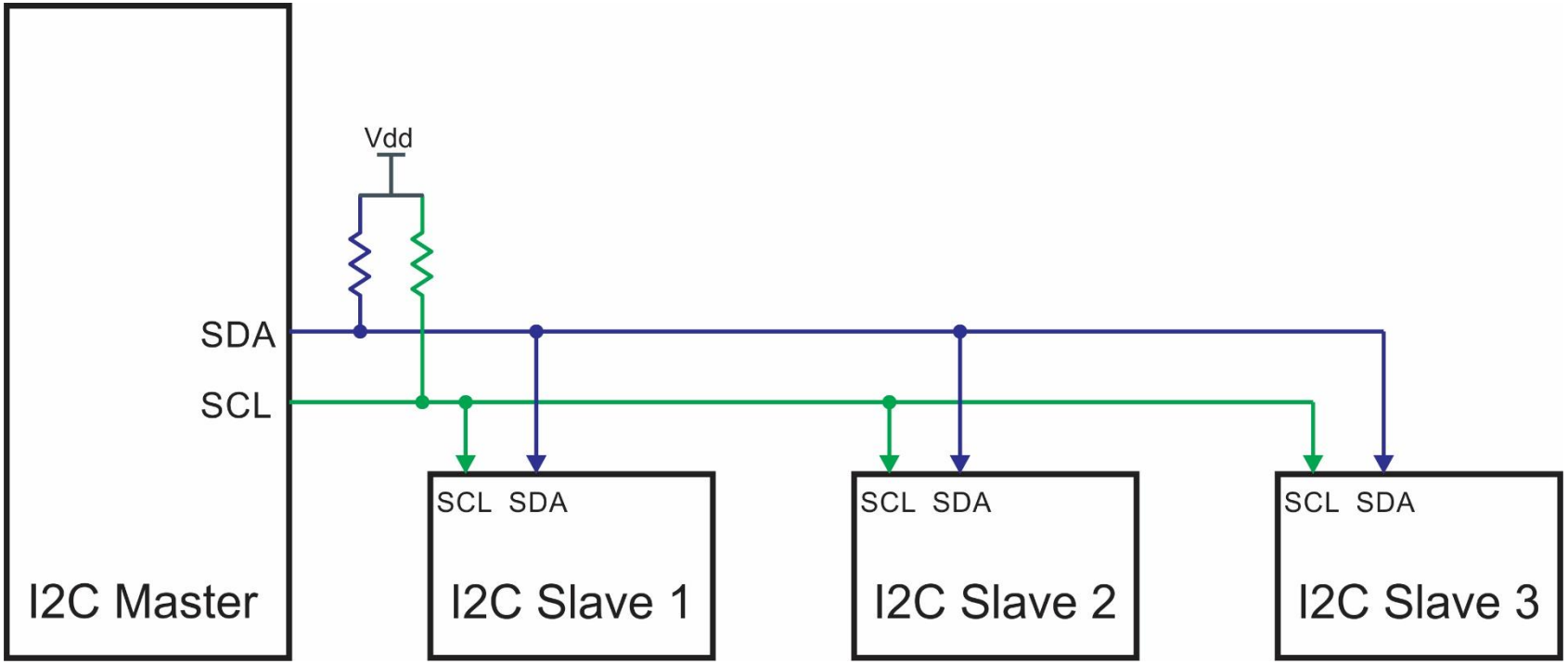
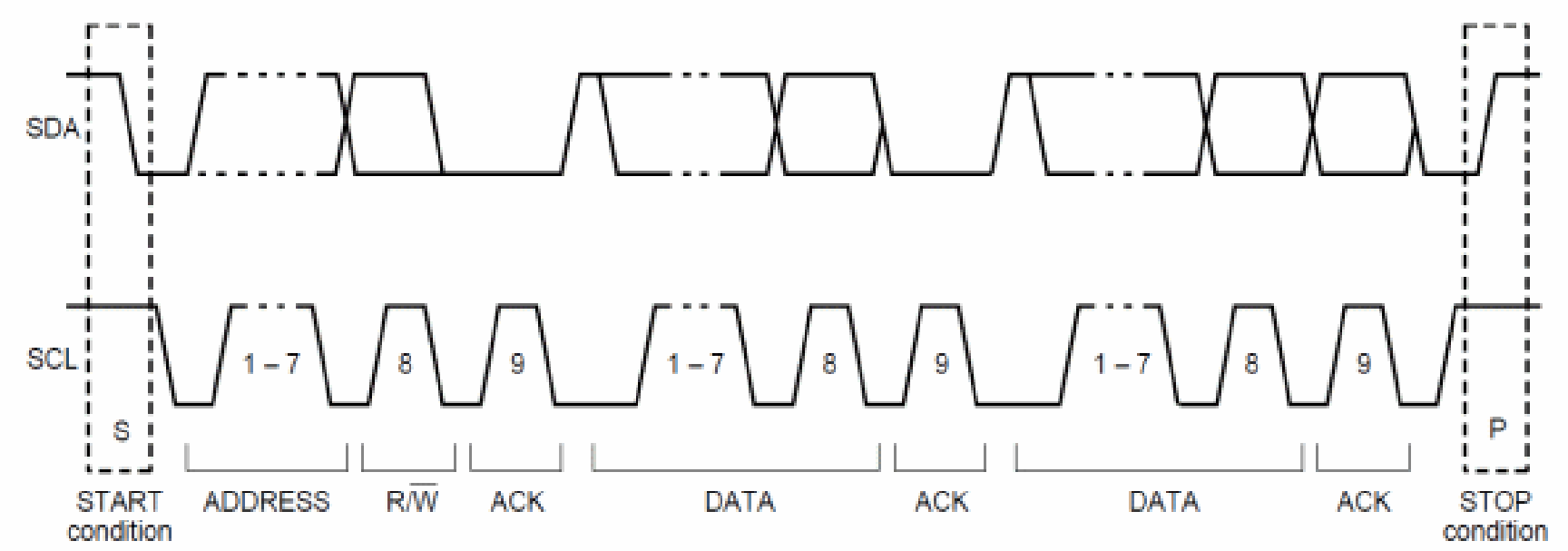
I2C – Inter-Integrated Circuit

- Developed by Philips (NXP) in 1982
- 2 Wire Synchronous Serial (Half-Duplex)
- Bidirectional Open Collector Bus
- Master / Slave (Multi-Master)
- Master Initiates All Communication
- Up to 5Mb/s (100kb/s & 400kb/s common)
- Unique 7b or 10b address for Each Device

I2C Bus Connection



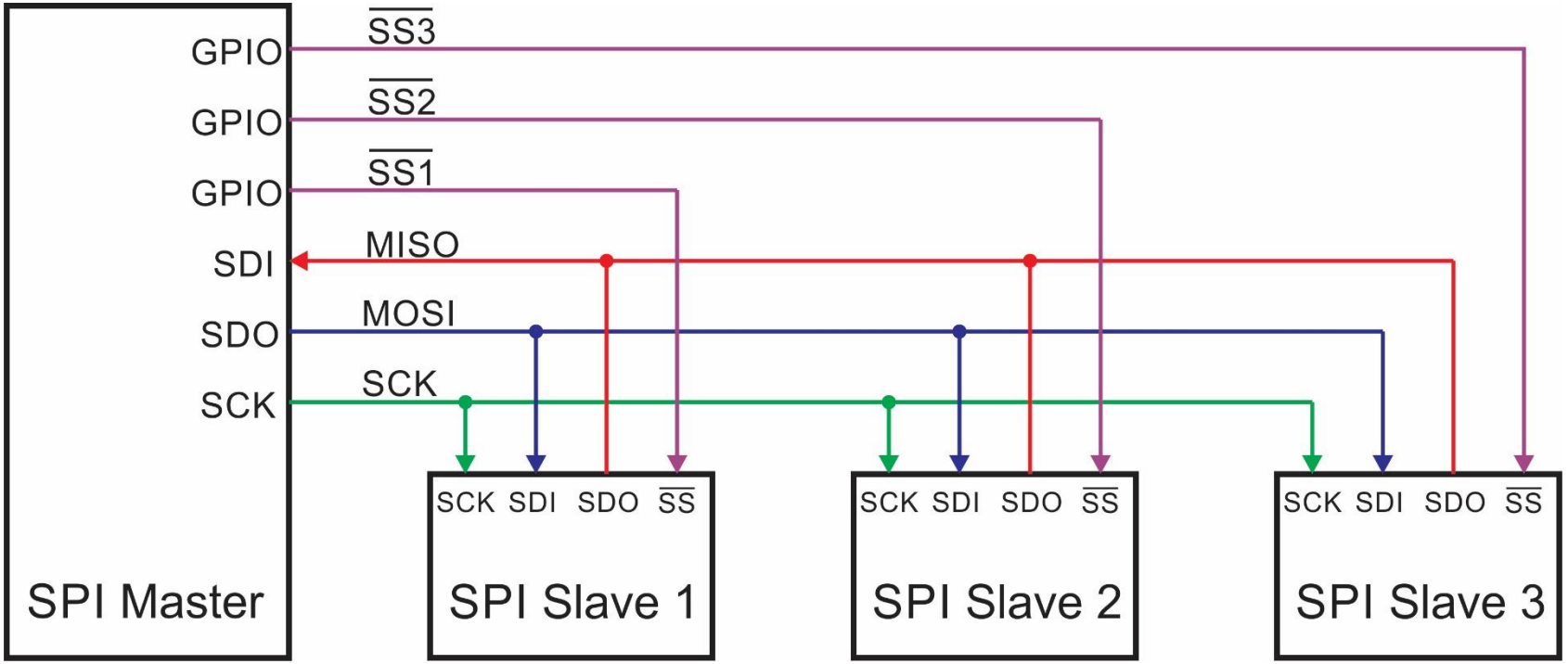
I2C Data Transfer



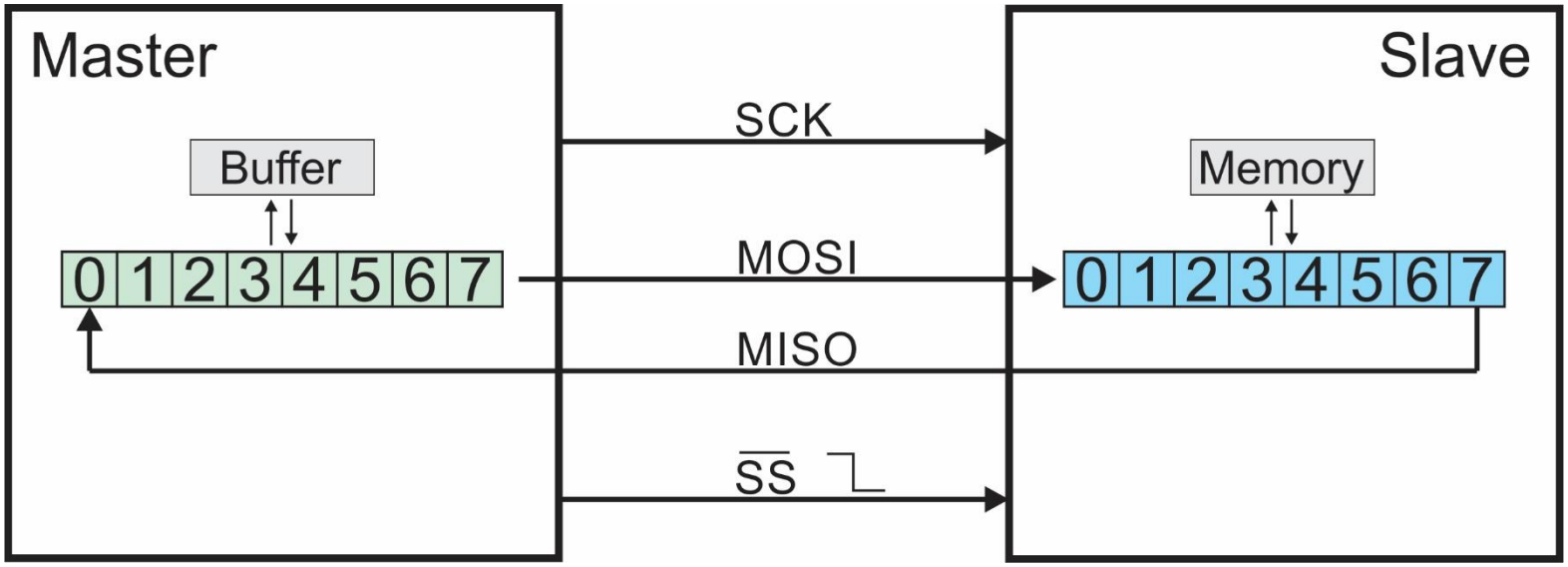
SPI – Serial Peripheral Interface

- Developed by Motorola (NXP) in 1987
- 3 Wire + nSS Serial (Full-Duplex)
- Master / Slave Relationship
- Operates as a 16b Shift Register (8b + 8b)
- Capable of Very High Speed Data Transfers
- 4 Modes for Clock Polarity and Phase
- No Formal Standard (many variations)

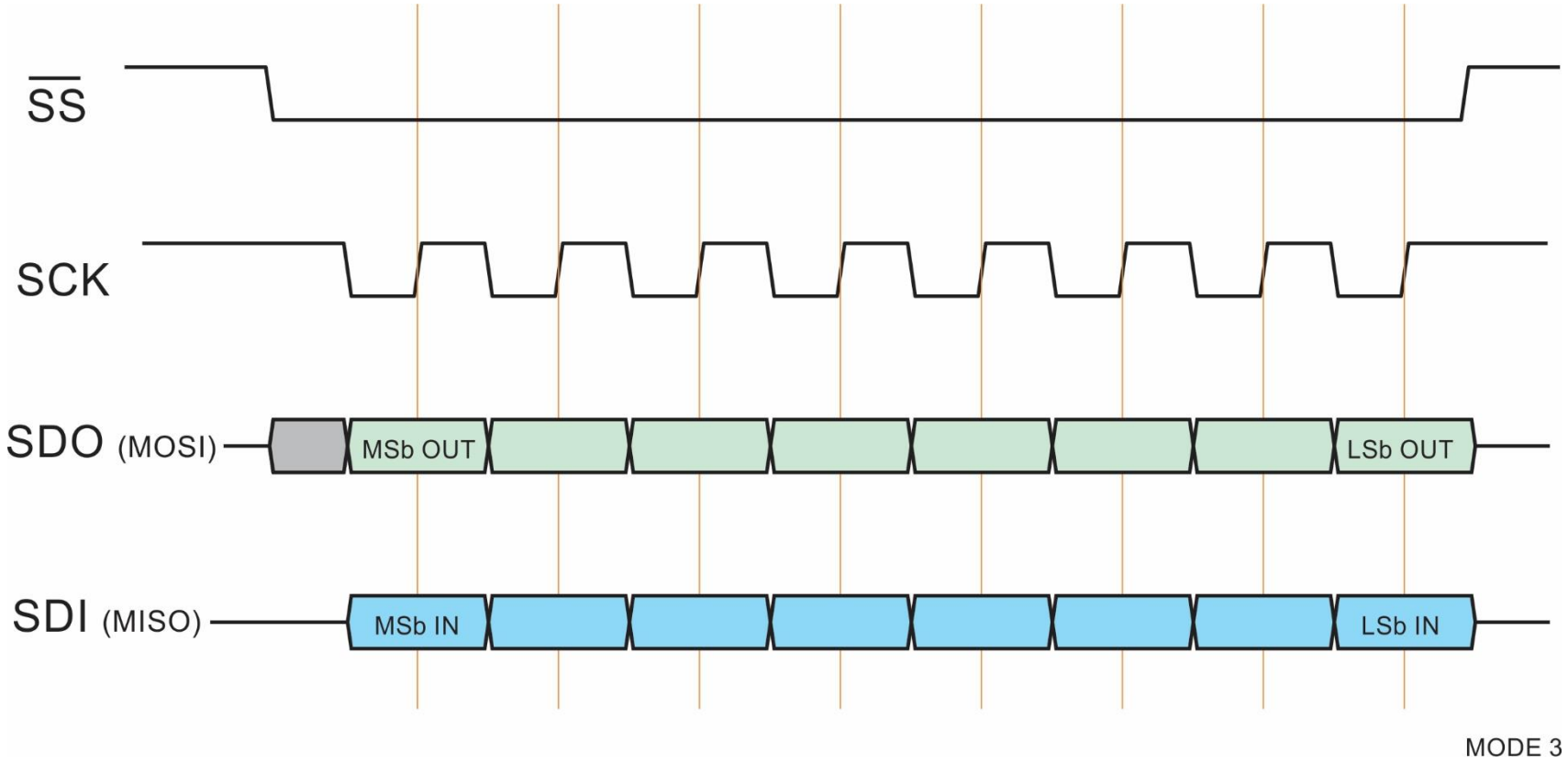
SPI Bus Connection



SPI – Shift Register



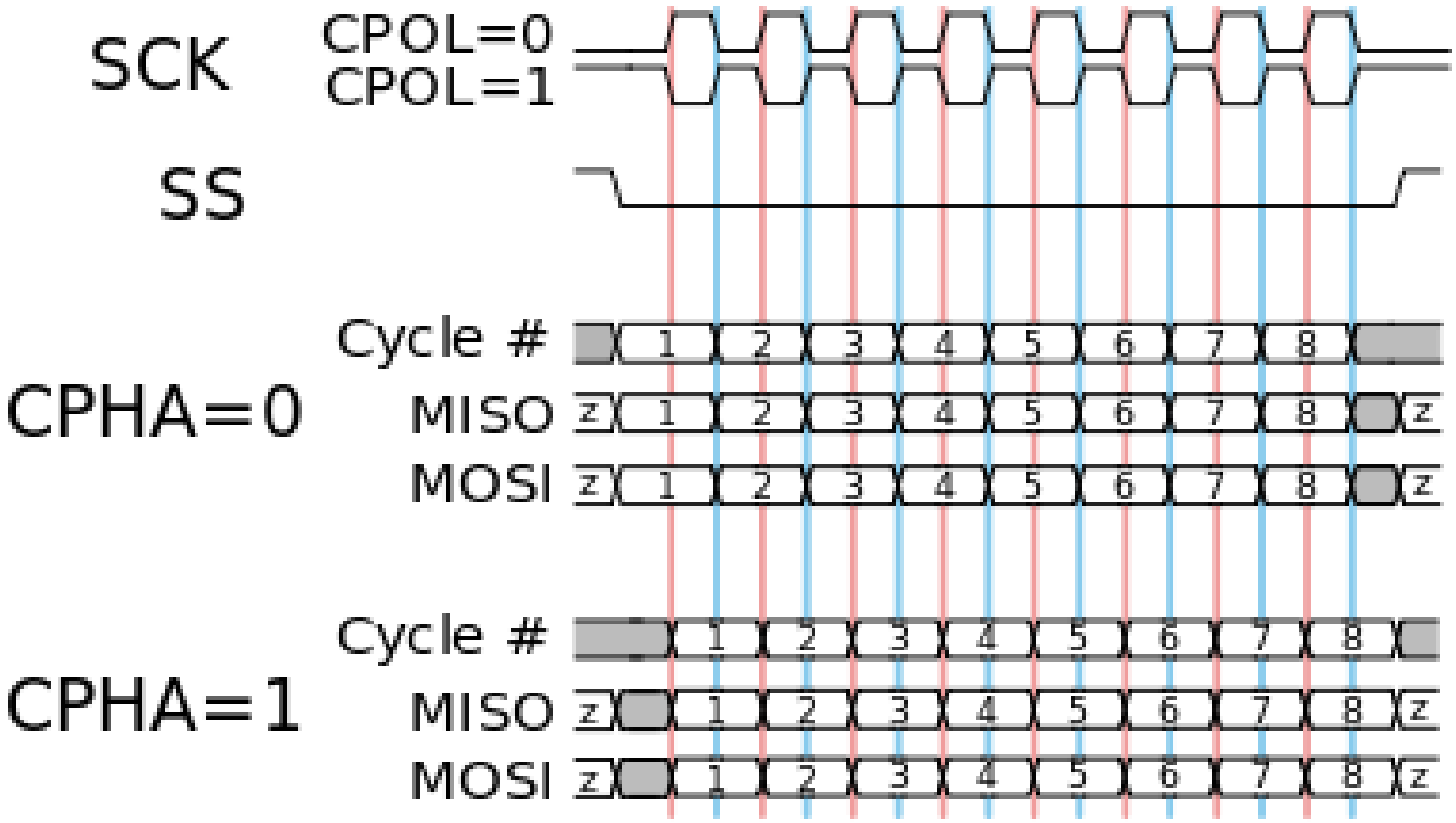
SPI – Data Transfer



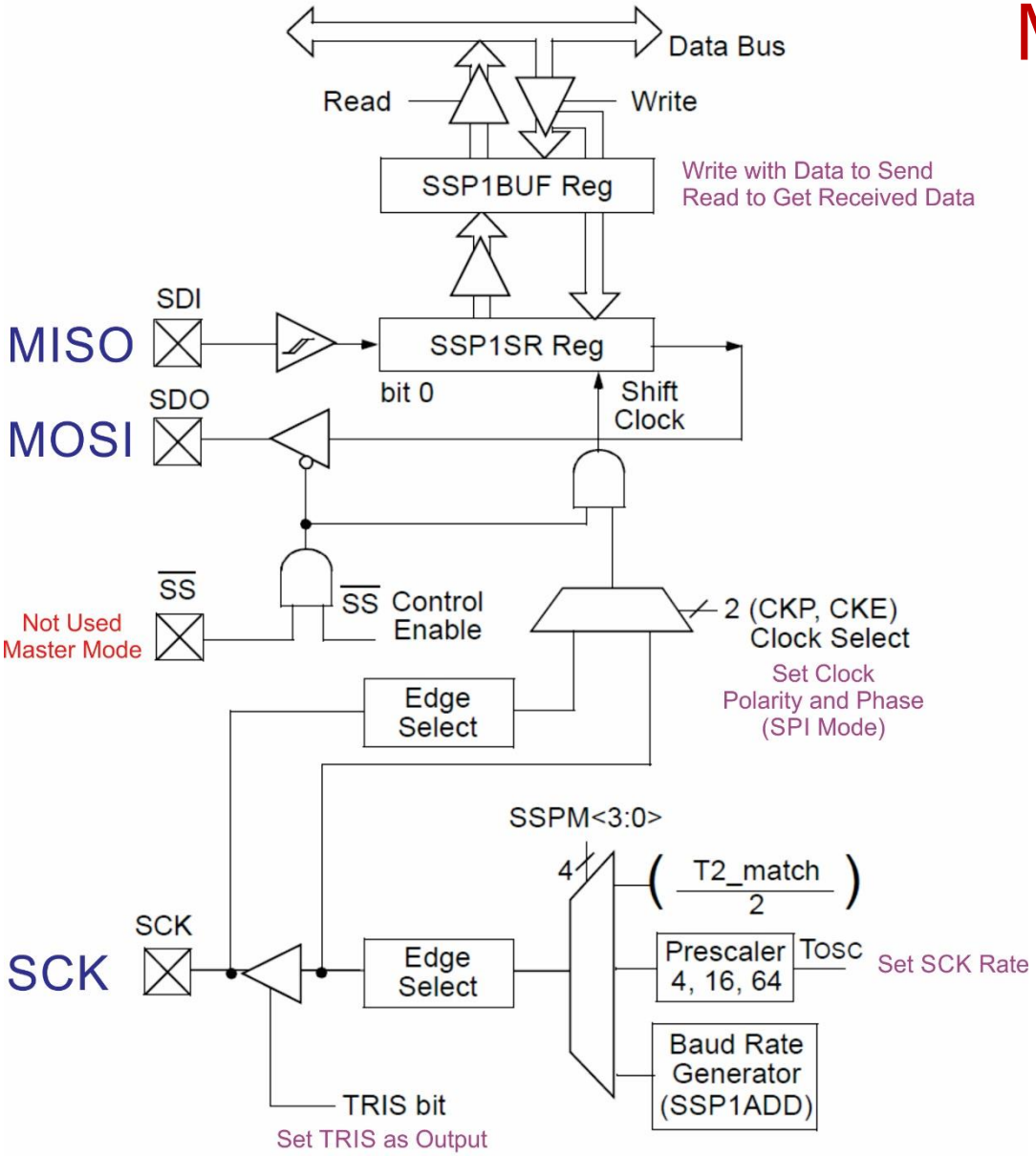
SPI

Clock Polarity and Phase

SPI Mode	Clock Polarity	Clock Phase
0	0	0
1	0	1
2	1	0
3	1	1



MSSP (SPI MODE)



SSP1STAT – Status

SSP1CON1 – Control 1

SSP1CON3 – Control 3
(slave settings)

SSP1BUF – Data Buffer

SSP1ADD – Address
(slave settings)

SSP1SR – Shift Register
(not accessible)

REGISTER 29-1: SSP1STAT: SSP STATUS REGISTER

R/W-0/0	R/W-0/0	R/HS/HC-0/0	R/HS/HC-0/0	R/HS/HC-0/0	R/HS/HC-0/0	R/HS/HC-0/0	R/HS/HC-0/0
SMP	CKE(1)	D/$\overline{A}$	P(2)	S(2)	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS/HC = Hardware set/clear

bit 7 **SMP:** SPI Data Input Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode
In I^2C™ Master or Slave mode:
1 = Slew rate control disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for High-Speed mode (400 kHz)

→ Set Input Sampling

bit 6 **CKE:** SPI Clock Edge Select bit (SPI mode only)(1)
In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state
In I^2C™ mode only:
1 = Enable input logic so that thresholds are compliant with SMBus specification
0 = Disable SMBus specific inputs

→ Set Active Clock Edge

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit (I^2C™ mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit(2)
(I^2C™ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

bit 3 **S:** Start bit (2)
(I^2C™ mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information (I^2C™ mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.
In I^2C™ Slave mode:
1 = Read
0 = Write
In I^2C™ Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

bit 1 **UA:** Update Address bit (10-bit I^2C™ mode only)
1 = Indicates that the user needs to update the address in the SSP1ADD register
0 = Address does not need to be updated

bit 0 **BF:** Buffer Full Status bit
Receive (SPI and I^2C™ modes):
1 = Receive complete, SSP1BUF is full
0 = Receive not complete, SSP1BUF is empty
Transmit (I^2C™ mode only):
1 = Data transmit in progress (does not include the $\overline{ACK}$ and Stop bits), SSP1BUF is full
0 = Data transmit complete (does not include the $\overline{ACK}$ and Stop bits), SSP1BUF is empty

→ Buffer Full Status Flag (Exchange Done)

Note 1: Polarity of clock state is set by the CKP bit of the SSP1CON register.
2: This bit is cleared on Reset and when SSPEN is cleared.

REGISTER 29-2: SSP1CON1: SSP CONTROL REGISTER 1

R/C/HS-0/0	R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPOV(1)	SSPEN	CKP	SSPM<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets	
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware	C = User cleared

bit 7 **WCOL:** Write Collision Detect bit (Transmit mode only)
1 = The SSP1BUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

→ Clear WCOL

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)
In SPI mode:
1 = A new byte is received while the SSP1BUF register is still holding the previous data. In case of overflow, the data in SSP1SR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSP1BUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSP1BUF register (must be cleared in software).
0 = No overflow
In I²C mode:
1 = A byte is received while the SSP1BUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
0 = No overflow

bit 5 **SSPEN:** Synchronous Serial Port Enable bit
In both modes, when enabled, the following pins must be properly configured as input or output
In SPI mode:
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as the source of the serial port pins(2)
0 = Disables serial port and configures these pins as I/O port pins
In I²C™ mode:
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins(3)
0 = Disables serial port and configures these pins as I/O port pins

→ Enable SPI

bit 4 **CKP:** Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I²C™ Slave mode:
SCL release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
In I²C™ Master mode:
Unused in this mode

→ Set Clock Polarity

bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits
1111 = I²C™ Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I²C™ Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1101 = Reserved
1100 = Reserved
1011 = I²C™ firmware controlled Master mode (slave idle)
1010 = SPI Master mode, clock = FOSC/(4 * (SSP1ADD+1))(5)
1001 = Reserved
1000 = I²C™ Master mode, clock = FOSC / (4 * (SSP1ADD+1))(4)
0111 = I²C™ Slave mode, 10-bit address
0110 = I²C™ Slave mode, 7-bit address
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0011 = SPI Master mode, clock = T2_match/2
0010 = SPI Master mode, clock = FOSC/64
0001 = SPI Master mode, clock = FOSC/16
0000 = SPI Master mode, clock = FOSC/4

→ Master Mode & Bus Speed

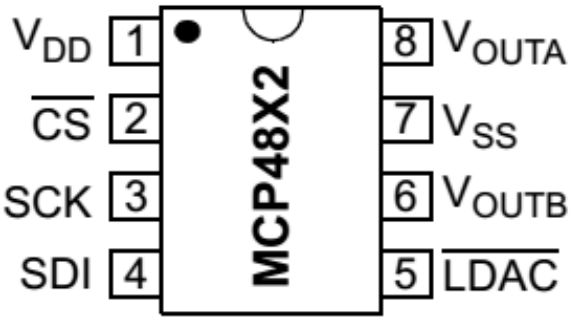
TRIS setup for SPI

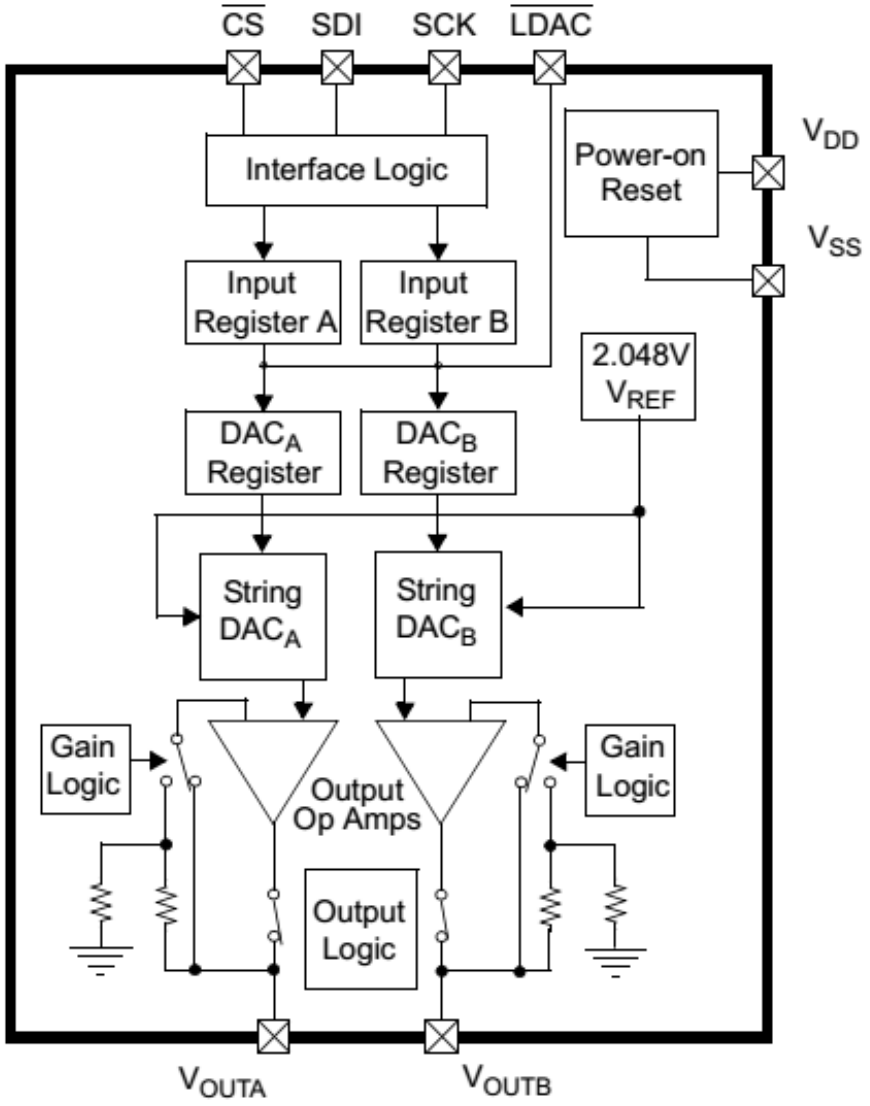
- SDI (MISO) – Set TRIS bit
- SDO (MOSI) – Clear TRIS bit
- SCK (Master Mode) – Clear TRIS bit
- nSS (Master Mode) – GPIO Clear TRIS

- SCK (Slave Mode) – Set TRIS bit
- nSS (Slave Mode) – Set TRIS

MCP4822 – 12b DAC

- SPI Interface (20MHz)
- Rail-to-Rail Output
- 2.048V Internal Voltage Ref
- 2.7V to 5.5V Operation





MCP4822 – Command Register

REGISTER 5-1: WRITE COMMAND REGISTER FOR MCP4822 (12-BIT DAC)

W-x	W-x	W-x	W-0	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
$\overline{A/B}$	—	$\overline{GA}$	$\overline{SHDN}$	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
bit 15															bit 0

bit 15 **$\overline{A/B}$:** DAC_A or DAC_B Selection bit
1 = Write to DAC_B
0 = Write to DAC_A

bit 14 — Don't Care

bit 13 **$\overline{GA}$:** Output Gain Selection bit
1 = 1x ($V_{OUT} = V_{REF} * D/4096$)
0 = 2x ($V_{OUT} = 2 * V_{REF} * D/4096$), where internal V_{REF} = 2.048V.

bit 12 **$\overline{SHDN}$:** Output Shutdown Control bit
1 = Active mode operation. V_{OUT} is available.
0 = Shutdown the selected DAC channel. Analog output is not available at the channel that was shut down. V_{OUT} pin is connected to 500 kΩ (typical).