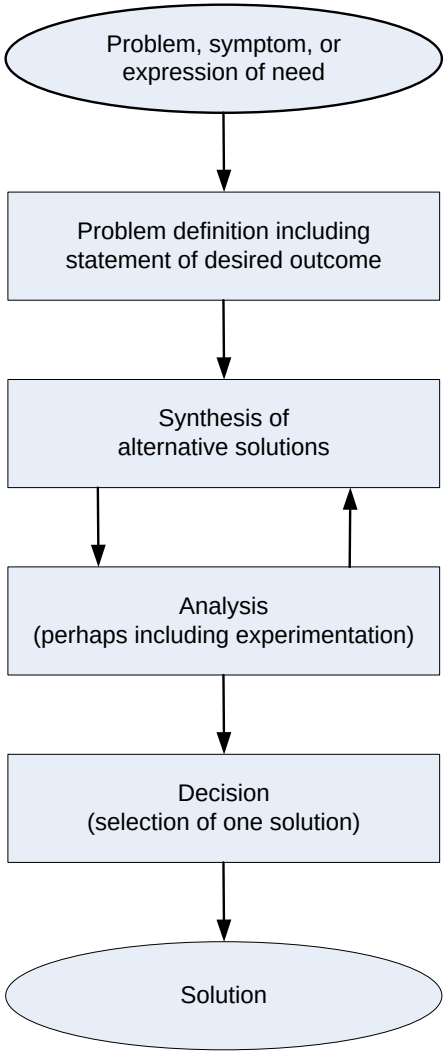
The Design Process
&
PIC Timers And Interrupts

ECE Senior Design

21 February 2018

The General Engineering Process



Synthesis: The putting together of parts or elements so as to form a whole.

Analysis: A separating or breaking up of any whole into its parts, especially with an examination of these parts to find out their nature, proportion, function, interrelationship, etc.

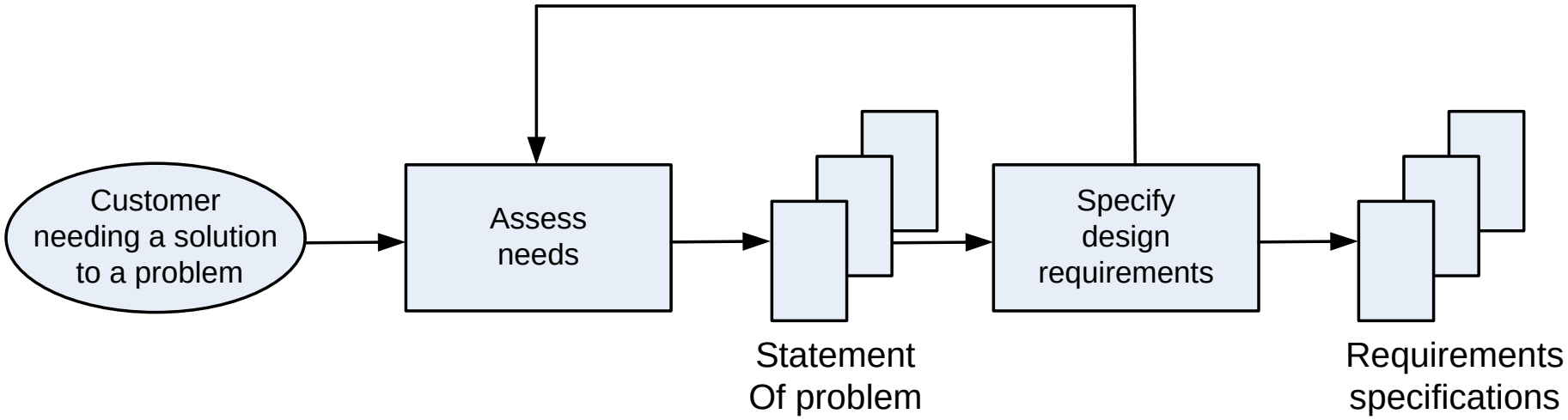
Requirements Analysis

(The Two Big Questions)

- What exactly is the design to accomplish?
- How will we know when we are done?

Developing a Requirements Specification

- Understand your Customer.
- Avoid a Search for Solutions!

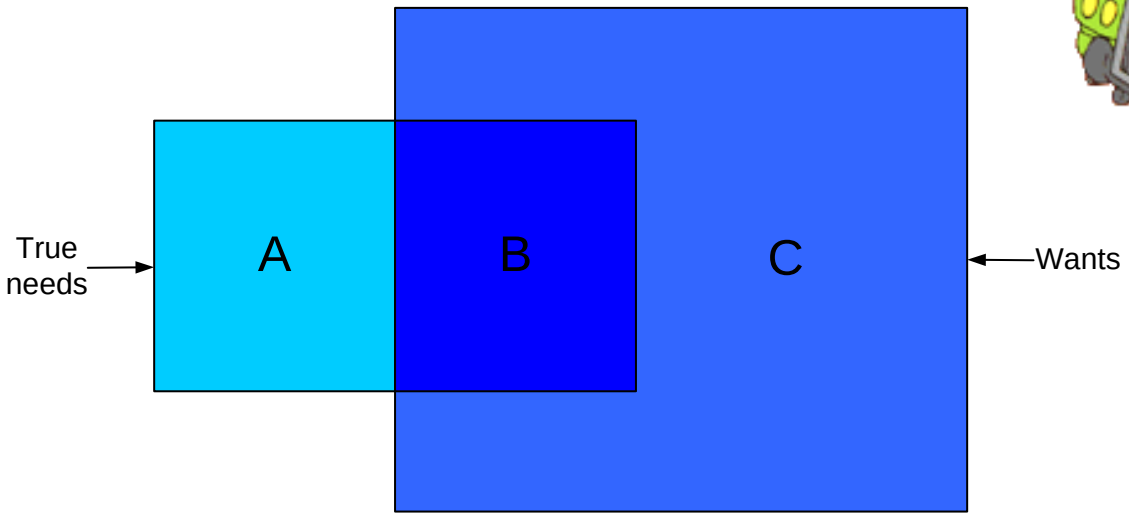


Purpose of Requirement Analysis

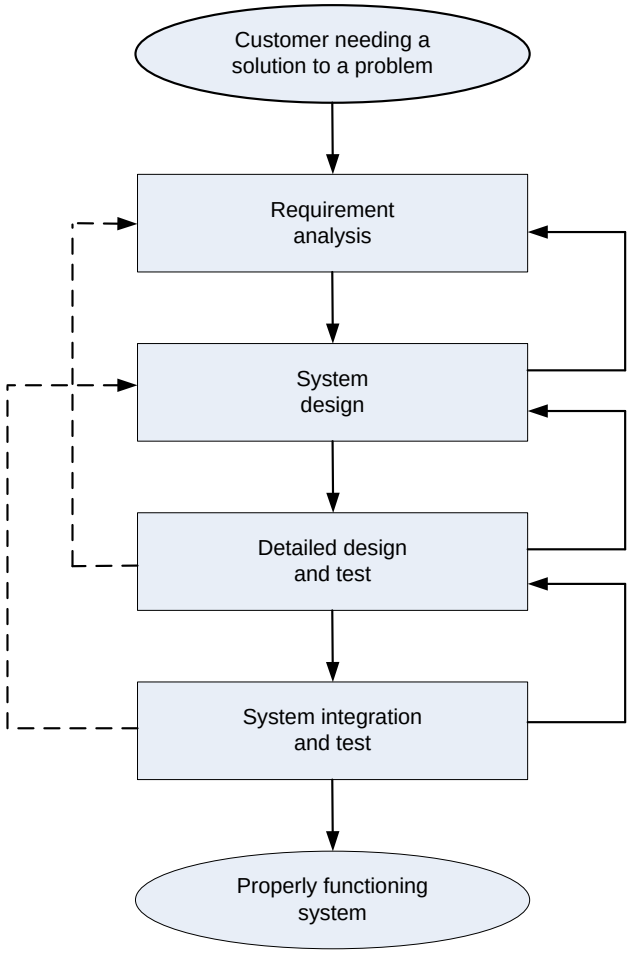
- Provides an benchmark for when a design is complete.
- Provides a “go, no-go” indicator for making decisions during the design process.
- Helps weed out overly ambitious and impractical design starts. *In many industries fewer than 10% of the design starts result in commercially viable products.*

Differentiate Needs and Wants

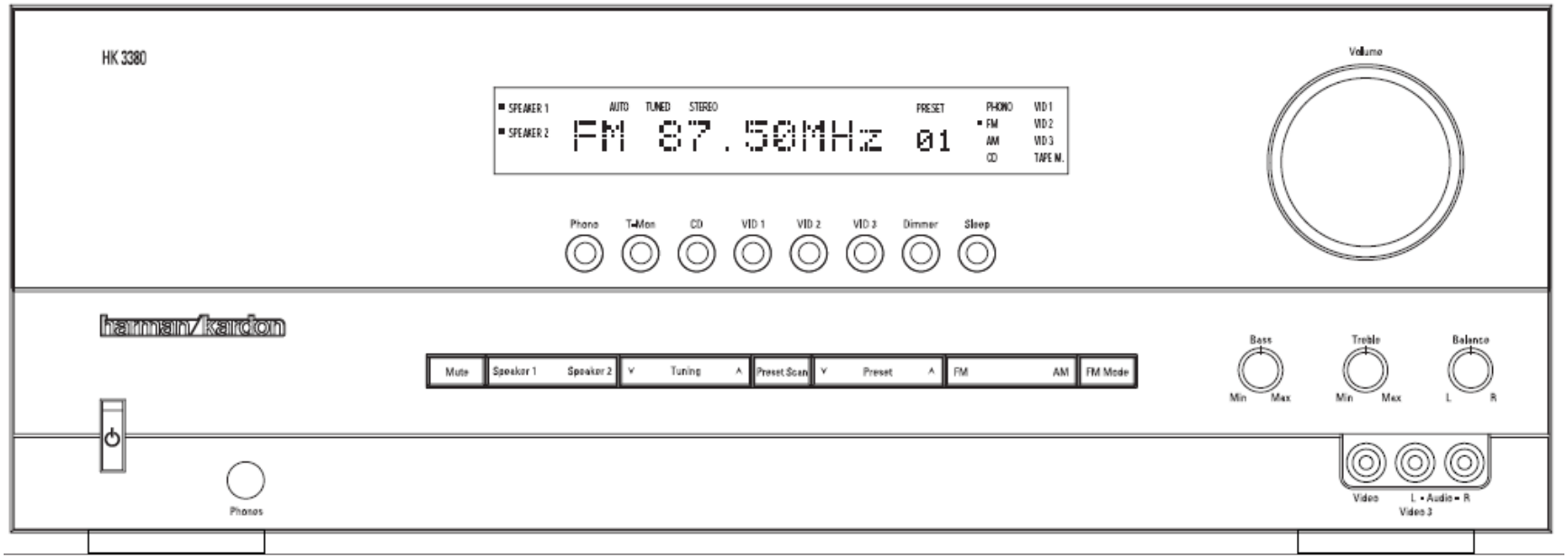
- Target “Requirements Specification” for needs not wants.



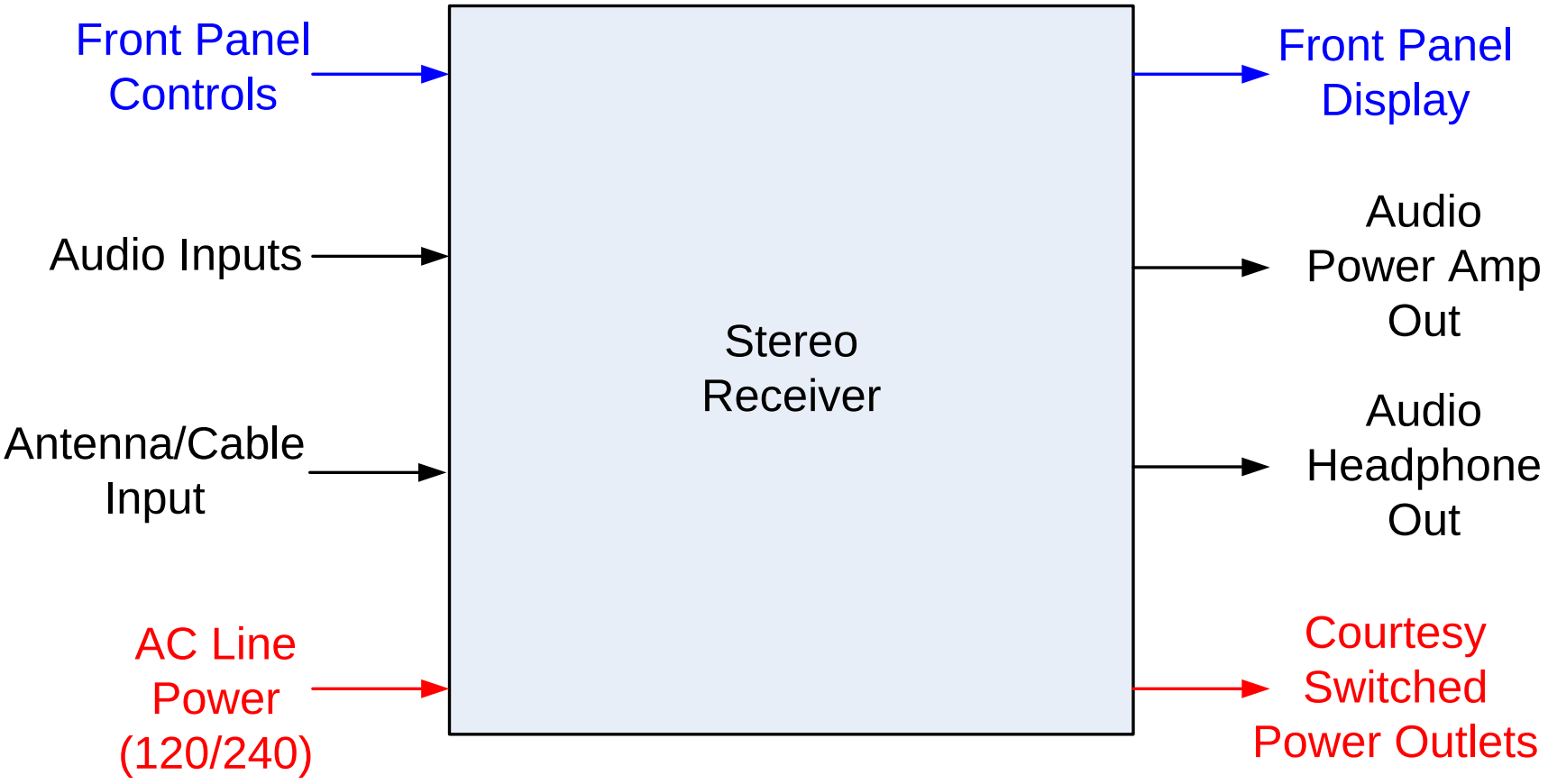
A Practical Design Methodology



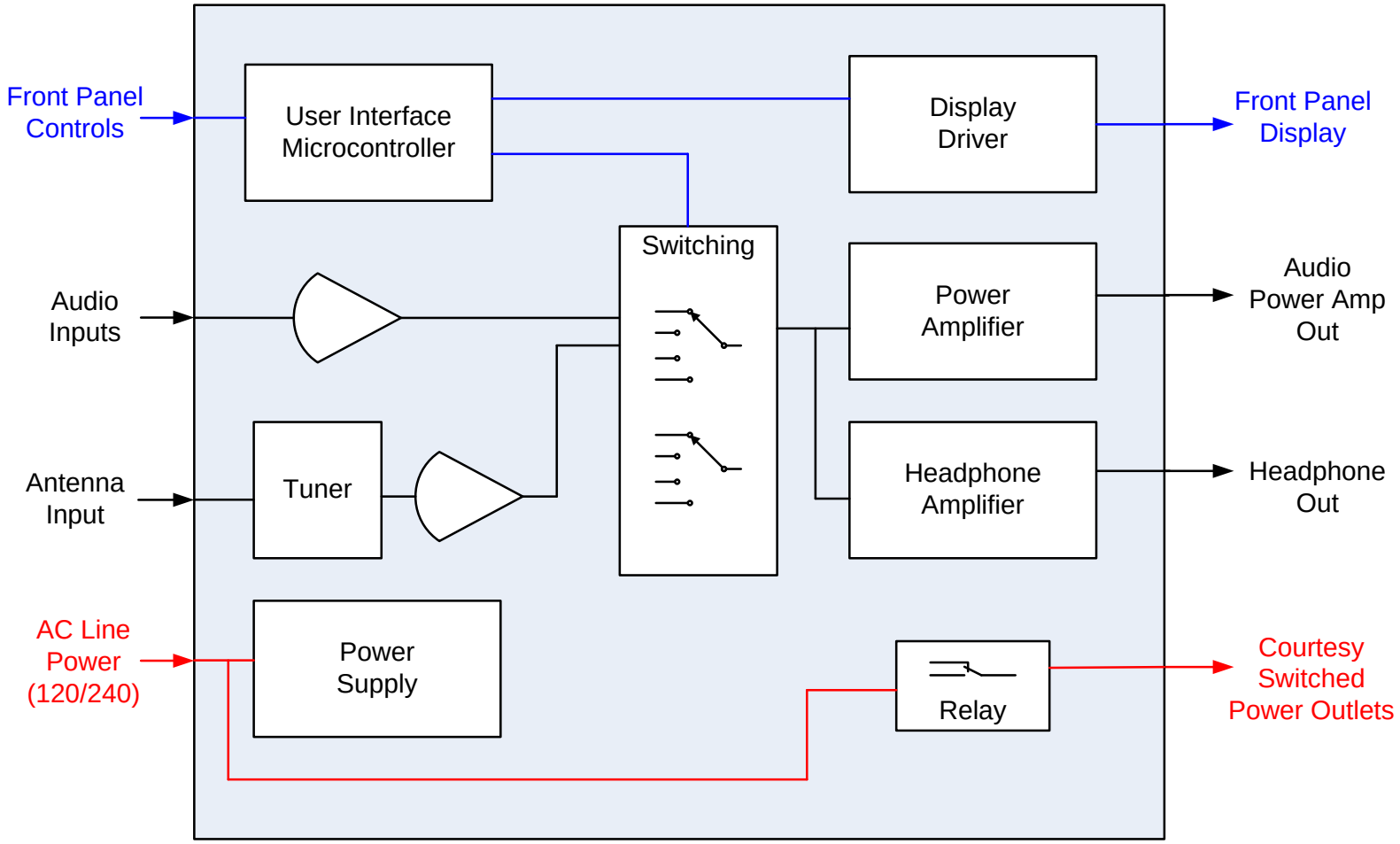
User Interface Mock-up



Input Output Analysis



Block Diagram



PIC Timers And Interrupts

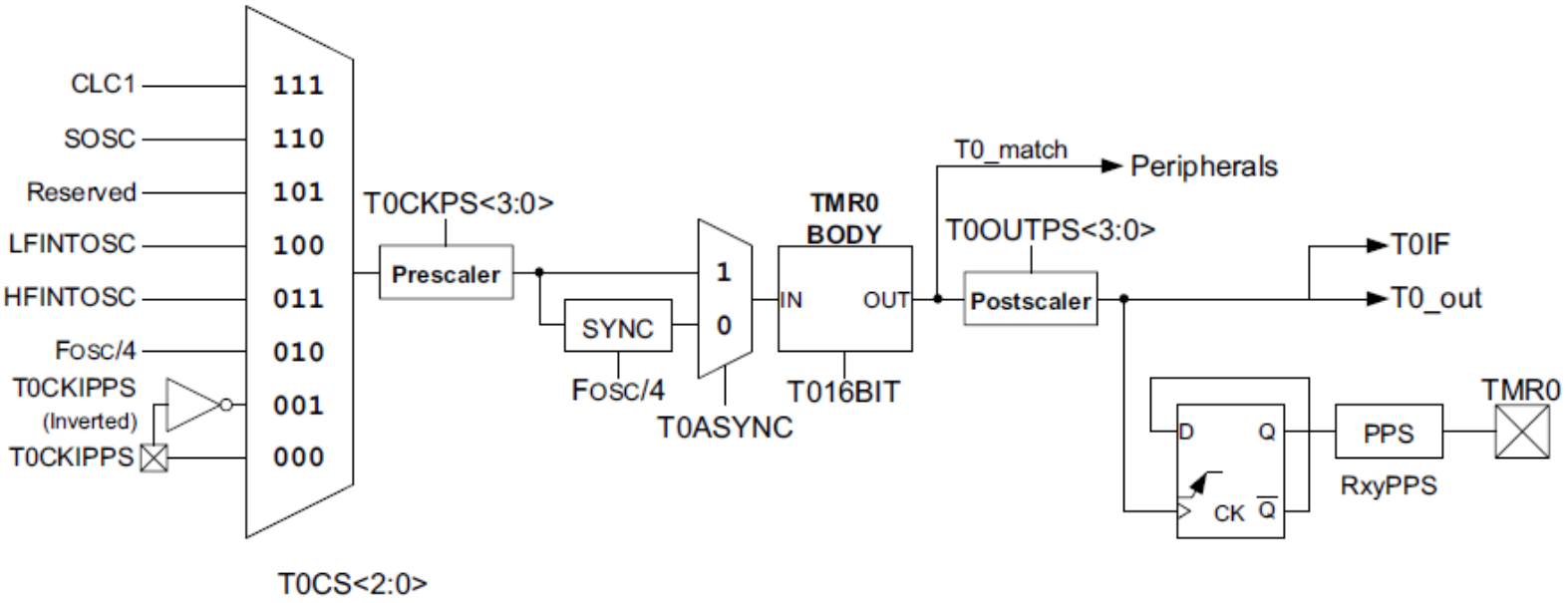
Timers in the PIC16F18324

- TMR0: 8/16-bit timer/counter with 15-bit Prescaler
- TMR1: 16-bit timer/counter with external enable
- TMR2: 8-bit timer with 8-bit Period Register
- Watchdog Timer
- NCO: Numerically Controlled Oscillator

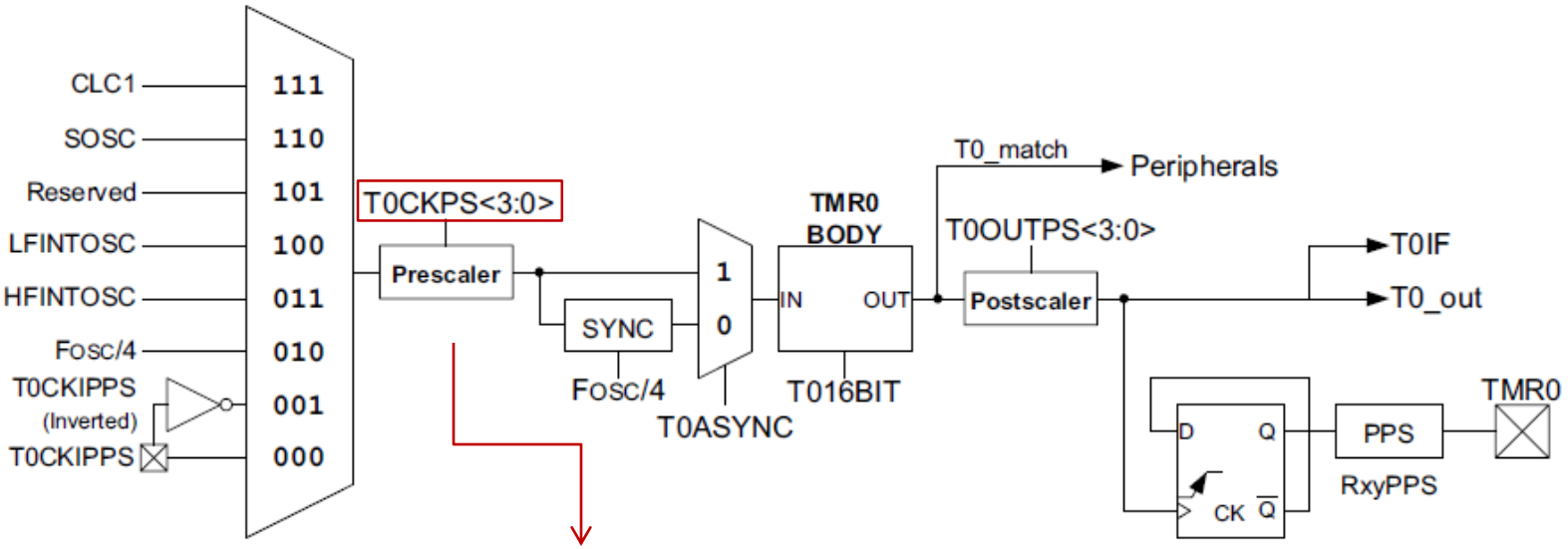
Timer0 Module (TMR0)

- 16-bit Timer/Counter
- 8-bit Timer/Counter with Programmable Period
- Selectable Clock Sources
- Programmable Prescaler and Postscaler
- Interrupt on Match or Overflow
- Output to I/O using PPS
- Operation is Sleep Mode

TIMER0 Block Diagram

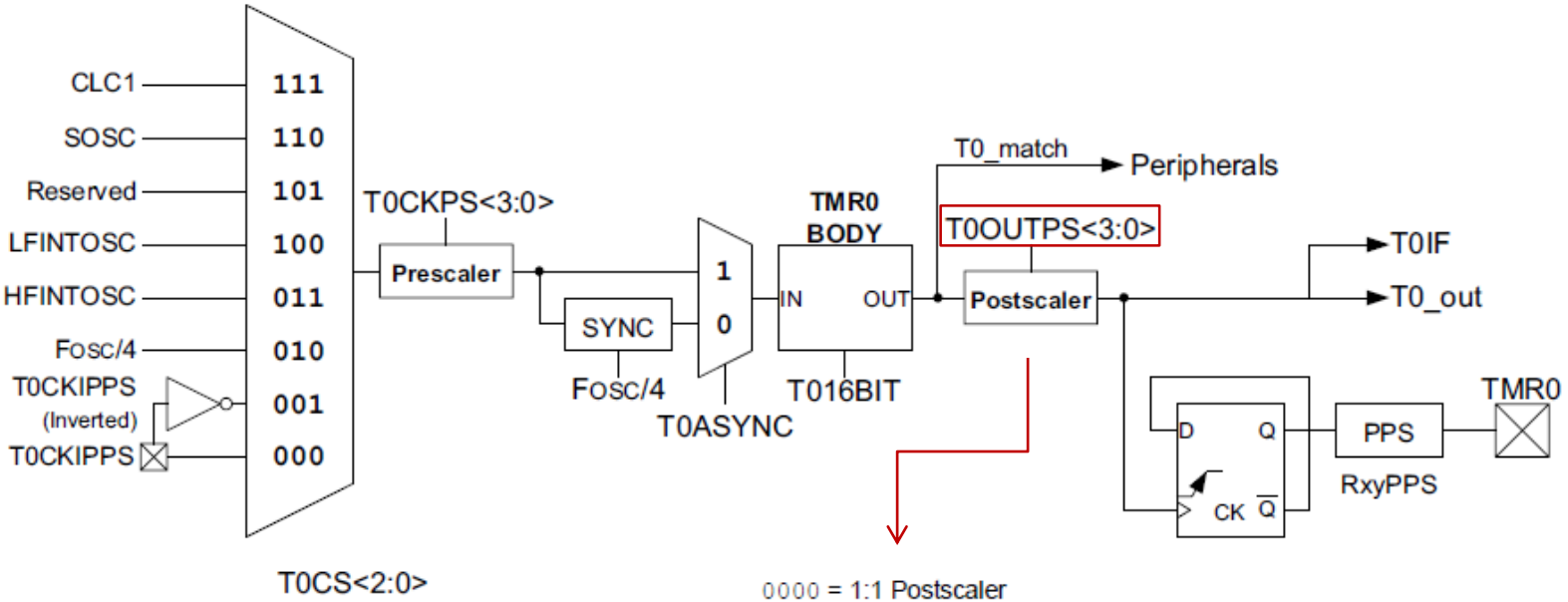


TIMER0 Block Diagram



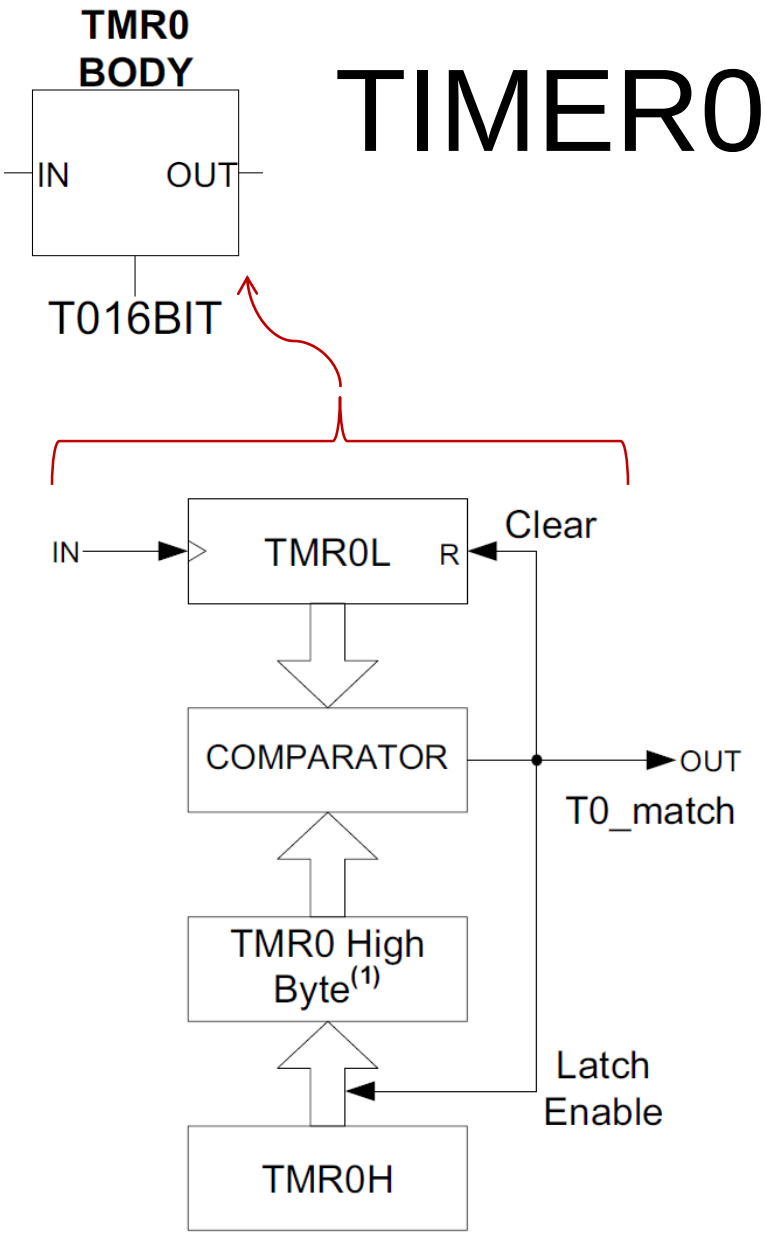
0000 = 1:1
0001 = 1:2
0010 = 1:4
0011 = 1:8
0100 = 1:16
0101 = 1:32
0110 = 1:64
0111 = 1:128
1000 = 1:256
1001 = 1:512
1010 = 1:1024
1011 = 1:2048
1100 = 1:4096
1101 = 1:8192
1110 = 1:16384
1111 = 1:32768

TIMER0 Block Diagram



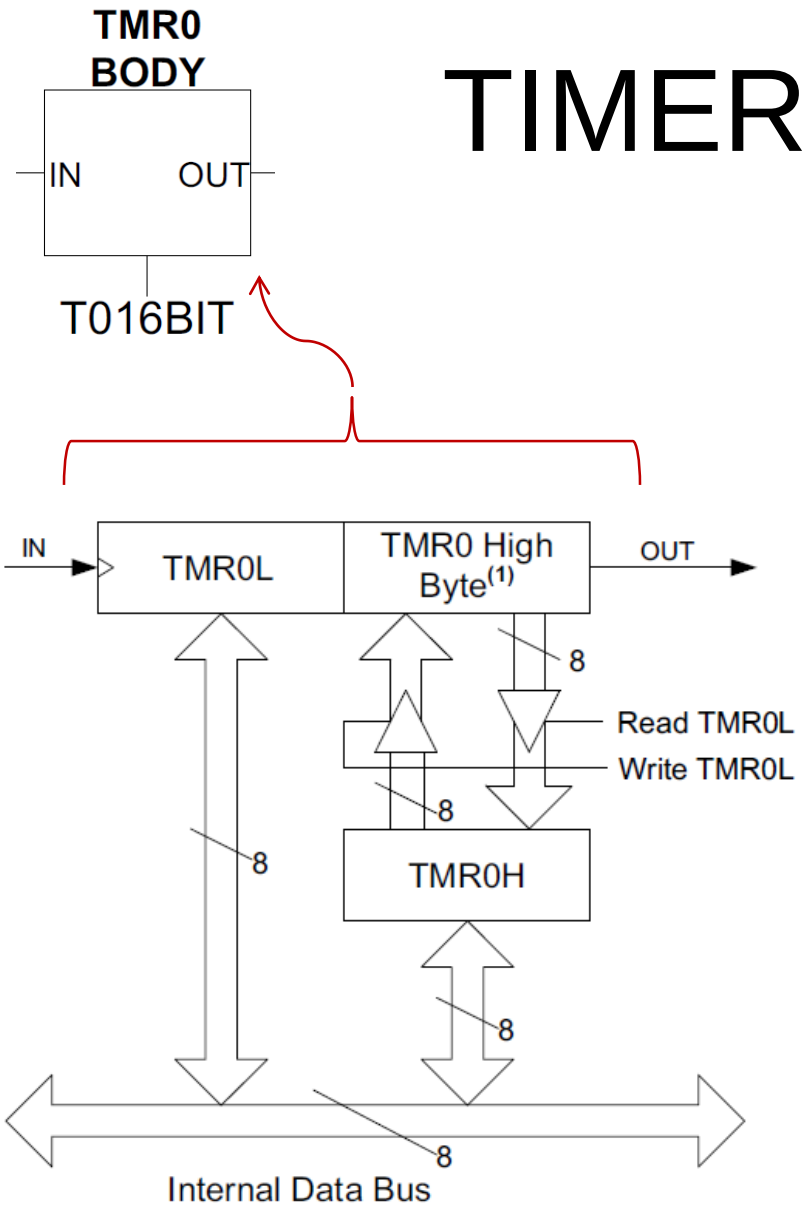
0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

TIMER0 – 8b Match Mode



- 8-bit Operation (T016BIT = 0)
- TMR0H is used as Period Buffer
- On Match of TMR0L and TMR0 High
  - Output Asserted for 1 Count
  - TMRL is Cleared
  - TMR0H is pushed into TMR0 High

TIMER0 – 16b Mode



- 16-bit Operation (T016BIT = 1)
- TMR0H Buffers the TMR0 High Byte
  - Updated on Read of TMR0L
  - Written on Write of TMR0L

T0CON0: TIMER0 CONTROL REGISTER 0

R/W-0/0	U-0	R-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **T0EN:** TMR0 Enable bit
1 = The module is enabled and operating
0 = The module is disabled and in the lowest-power mode

bit 6 **Unimplemented:** Read as '0'

bit 5 **T0OUT:** TMR0 Output (read-only) bit
TMR0 output bit

bit 4 **T016BIT:** TMR0 Operating as 16-bit Timer Select bit
1 = TMR0 is a 16-bit timer
0 = TMR0 is an 8-bit timer

bit 3-0 **T0OUTPS<3:0>:** TMR0 output postscaler (divider) select bits
0000 = 1:1 Postscaler
0001 = 1:2 Postscaler
0010 = 1:3 Postscaler
0011 = 1:4 Postscaler
0100 = 1:5 Postscaler
0101 = 1:6 Postscaler
0110 = 1:7 Postscaler
0111 = 1:8 Postscaler
1000 = 1:9 Postscaler
1001 = 1:10 Postscaler
1010 = 1:11 Postscaler
1011 = 1:12 Postscaler
1100 = 1:13 Postscaler
1101 = 1:14 Postscaler
1110 = 1:15 Postscaler
1111 = 1:16 Postscaler

T0CON1: TIMER0 CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
T0CS<2:0>			T0ASYNC	T0CKPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **T0CS<2:0>:**Timer0 Clock Source select bits
000 = T0CKIPPS (True)
001 = T0CKIPPS (Inverted)
010 = Fosc/4
011 = HFINTOSC
100 = LFINTOSC
101 = Reserved
110 = SOSC
111 = CLC1

bit 4 **T0ASYNC:** TMR0 Input Asynchronization Enable bit
1 = The input to the TMR0 counter is not synchronized to system clocks
0 = The input to the TMR0 counter is synchronized to Fosc/4

bit 3-0 **T0CKPS<3:0>:** Prescaler Rate Select bit
0000 = 1:1
0001 = 1:2
0010 = 1:4
0011 = 1:8
0100 = 1:16
0101 = 1:32
0110 = 1:64
0111 = 1:128
1000 = 1:256
1001 = 1:512
1010 = 1:1024
1011 = 1:2048
1100 = 1:4096
1101 = 1:8192
1110 = 1:16384
1111 = 1:32768

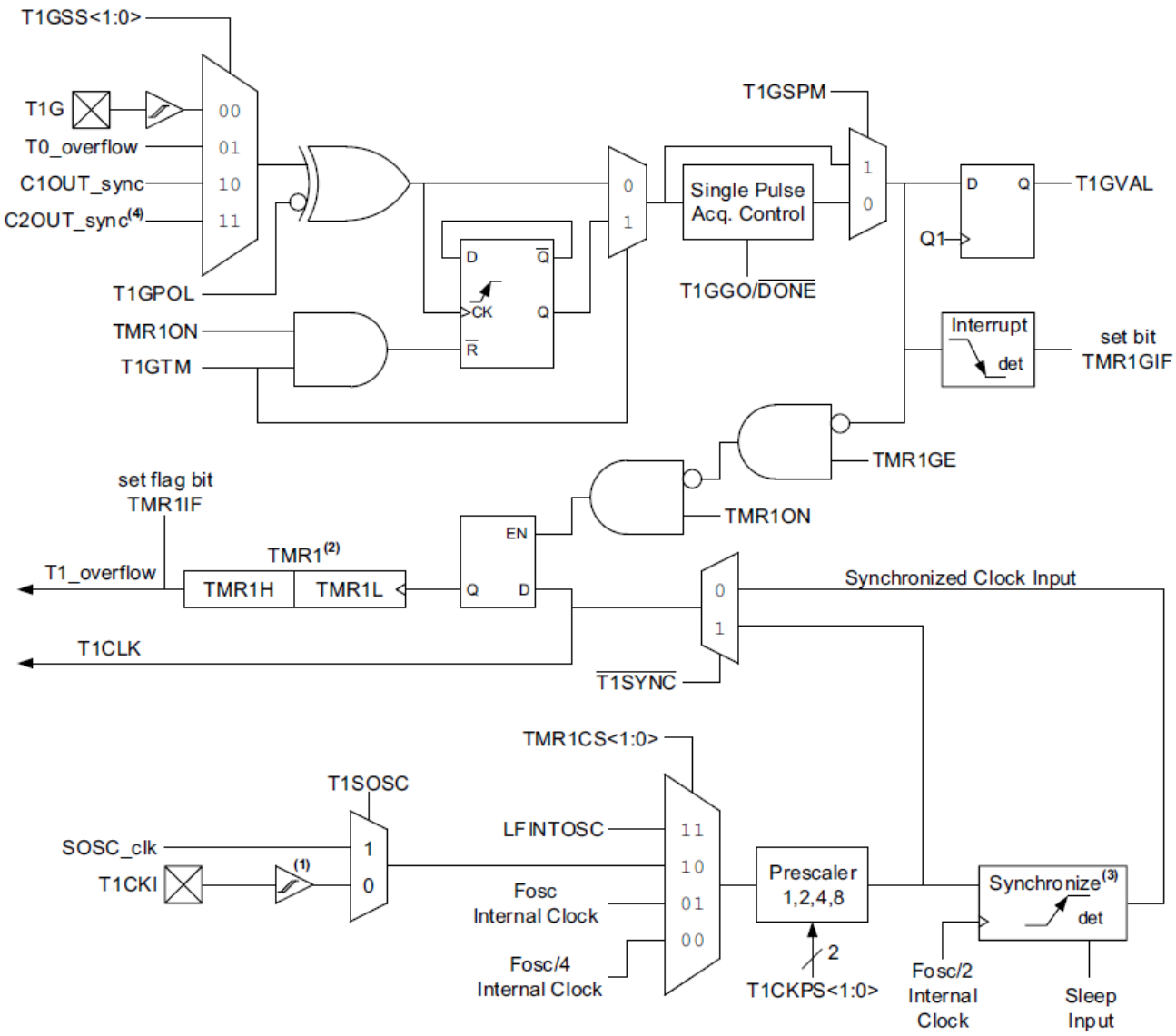
Registers Associated with TMR0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TRISA	—	—	TRISA5	TRISA4	—(2)	TRISA2	TRISA1	TRISA0	129
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	130
TRISC(1)	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	135
ANSELC(1)	—	—	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	136
TMR0L	TMR0<7:0>								250
TMR0H	TMR0<15:8>								250
T0CON0	T0EN	—	T0OUT	T016BIT	T0OUTPS<3:0>				251
T0CON1	T0CS<2:0>			T0ASYNC	T0CKPS<3:0>				252
T0CKIPPS	—	—	—	T0CKIPPS<4:0>					140
TMR0PPS	—	—	—	TMR0PPS<4:0>					250
ADACT	—	—	—	—	ADACT<3:0>				219
CLCxSELy	—	—	—	LCxDyS<4:0>					202
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		263
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	87
PIR0	—	—	TMR0IF	IOCIF	—	—	—	INTF	93
PIE0	—	—	TMR0IE	IOCIE	—	—	—	INTE	88

Timer1 Module (TMR1)

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock select
- 2-bit Prescaler - Divide by 1, 2, 4 or 8
- Gate count enable from external pin
- Interrupt on overflow from 0xFFFF to 0x0000
- Wake-Up on Overflow – External Osc.

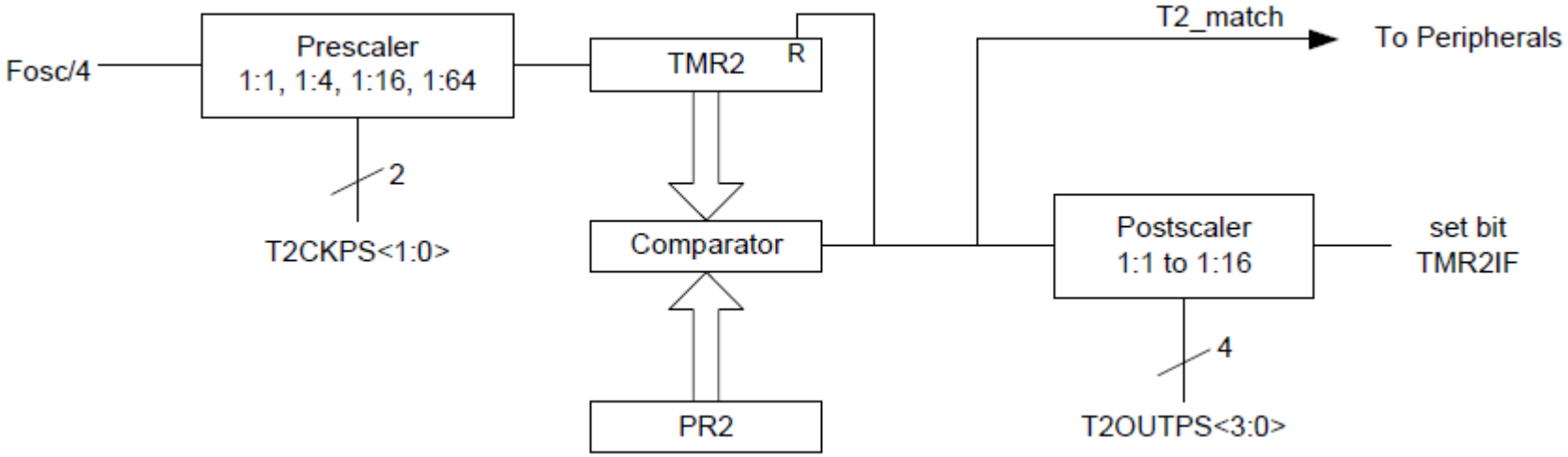
TMR1 Block Diagram



Timer2 Module (TMR2)

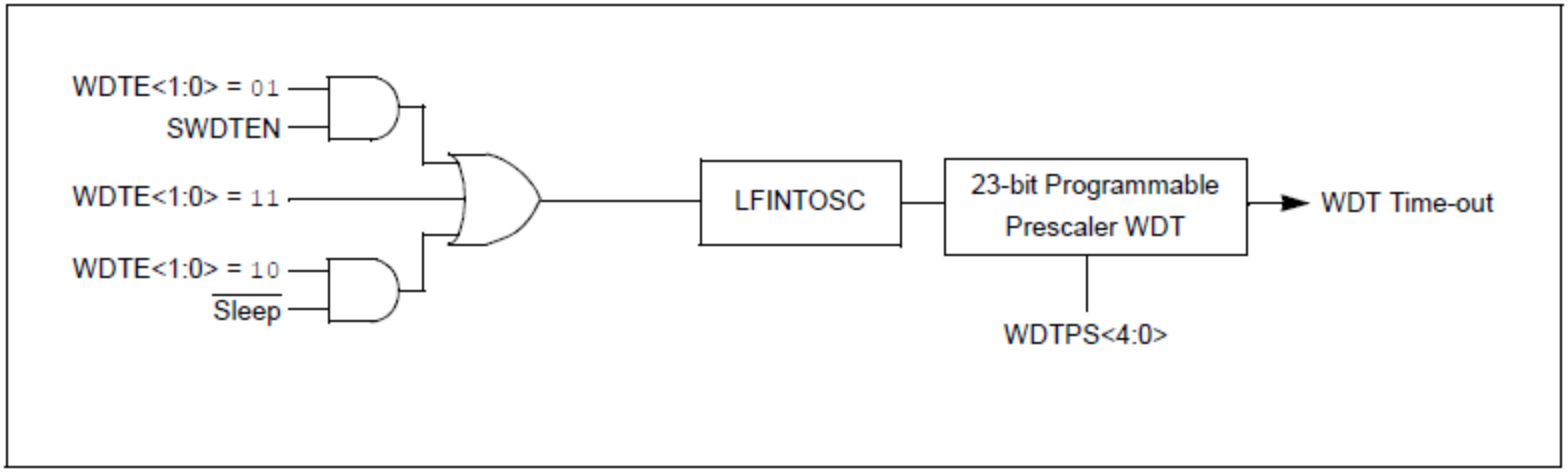
- 8-bit timer register (TMR2)
- 8-bit period register (PR2)
- Prescaler for (1:1, 1:4, 1:16 and 1:64)
- 4-bit Postscaler (1:1 to 1:16)
- Interrupt on TMR2 match with PR2
- Used for PWM (CCP Module)

TMR2 Block Diagram

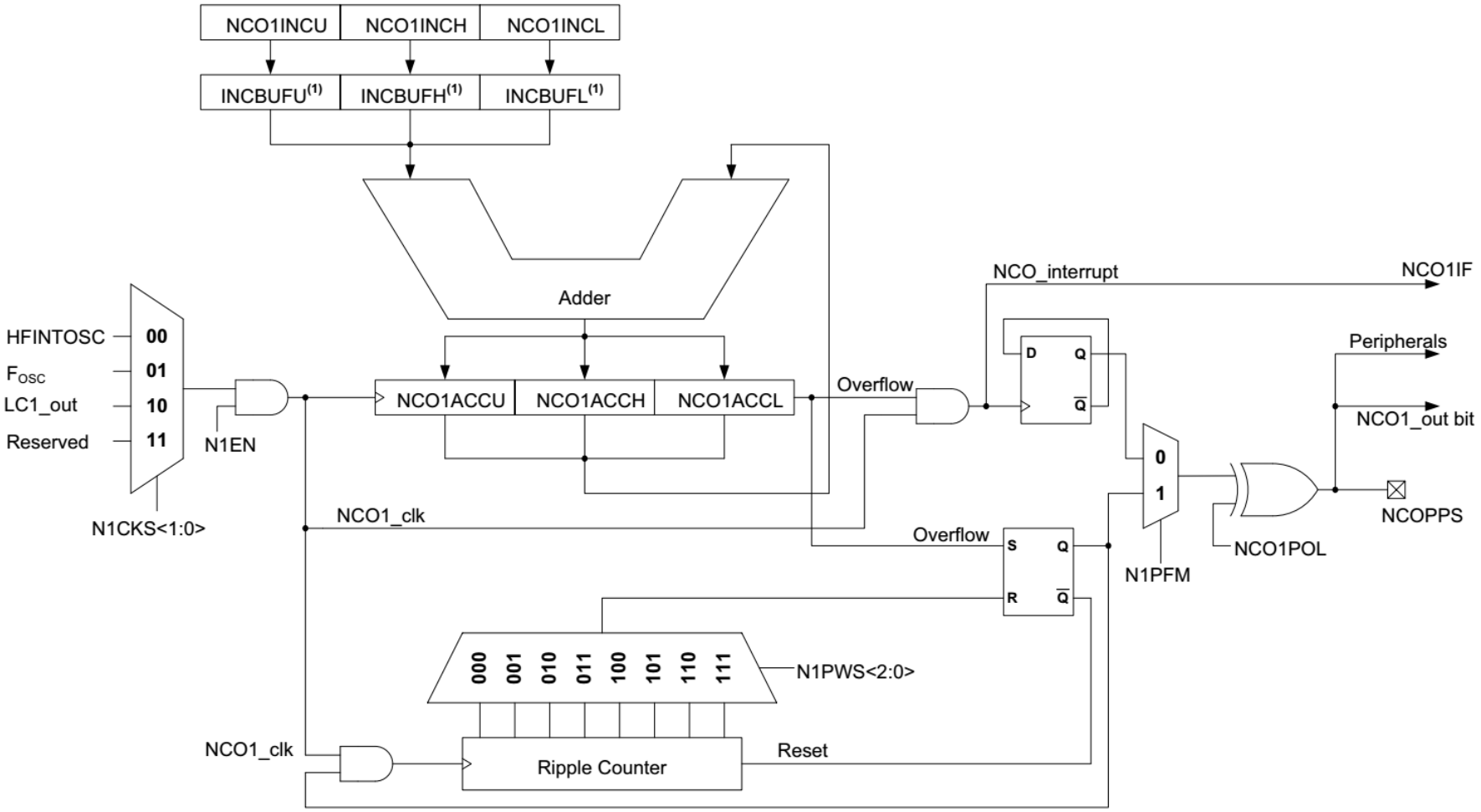


Watchdog Timer

- Independent clock source
- Timeout from 1ms to 256 seconds
- Can operate in Sleep



Numerically Controlled Oscillator



Commonly Used Interrupt Sources

- INT Pin (asyn edge-triggered)
- GPIO Pin Change
- TMR0 Overflow/Match
- TMR1 Overflow
- TMR2 Match
- Comparator Threshold Cross
- UART Receive Full
- I2C / SPI Data Receive Full

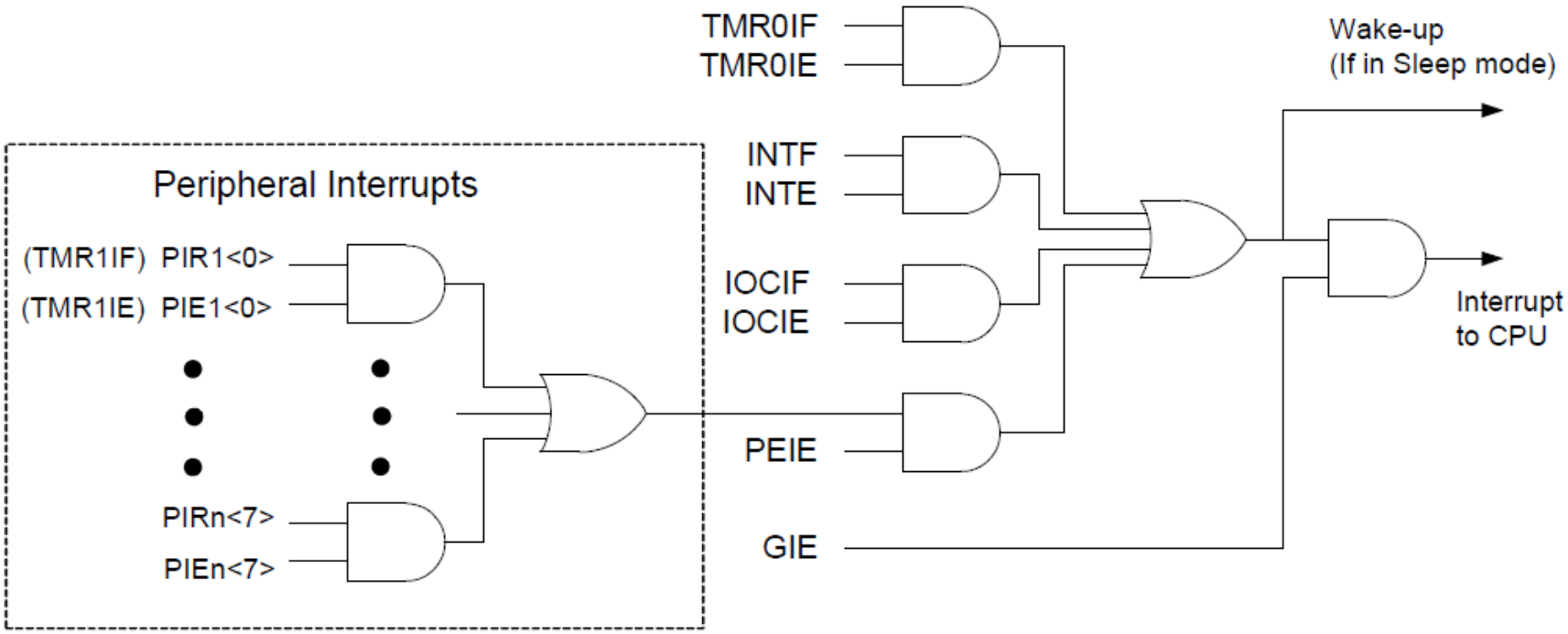
When an Interrupt Occurs

- GIE is cleared (no nested interrupts)
- Return address is pushed onto the stack
- Critical registers are saved to shadow
- The PC is loaded with 0x004

When an Interrupt Returns (RETFIE)

- Sets the GIE bit
- Critical registers are restored
- Pop return address from stack to PC

Interrupt Logic in the 16F18324



INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	U-0	R-1/1
GIE	PEIE	—	—	—	—	—	INTEDG
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5-1 **Unimplemented:** Read as '0'

bit 0 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

PIE0: PERIPHERAL INTERRUPT ENABLE REGISTER 0

U-0	U-0	R/W/HS-0/0	R-0	U-0	U-0	U-0	R/W/HS-0/0
—	—	TMR0IE	IOCIE	—	—	—	INTE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7-6 **Unimplemented**: Read as '0'

bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
- 1 = Enables the TMR0 interrupt
- 0 = Disables the TMR0 interrupt

bit 4 **IOCIE:** Interrupt-on-Change Interrupt Enable bit
- 1 = Enables the IOC change interrupt.
- 0 = Disables the IOC change interrupt.

bit 3-1 **Unimplemented**: Read as '0'

bit 0 **INTE:** INT External Interrupt Flag bit(1)
- 1 = Enables the INT external interrupt
- 0 = Disables the INT external interrupt

Note 1: The External Interrupt GPIO pin is selected by INTPPS (Register 12-1).

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

PIR0: PERIPHERAL INTERRUPT REQUEST REGISTER 0

U-0	U-0	R/W/HS-0/0	R-0	U-0	U-0	U-0	R/W/HS-0/0
—	—	TMR0IF	IOCIF	—	—	—	INTF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS= Hardware Set

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
- 1 = TMR0 register has overflowed (must be cleared in software)
- 0 = TMR0 register did not overflow

bit 4 **IOCIF:** Interrupt-on-Change Interrupt Flag bit (read-only)
- 1 = An enabled edge was detected by the IOC module. One of the IOCF bits is set.
- 0 = No enabled edge is was detected by the IOC module. None of the IOCF bits is set.

Pins are individually masked via IOCxP and IOCxN.

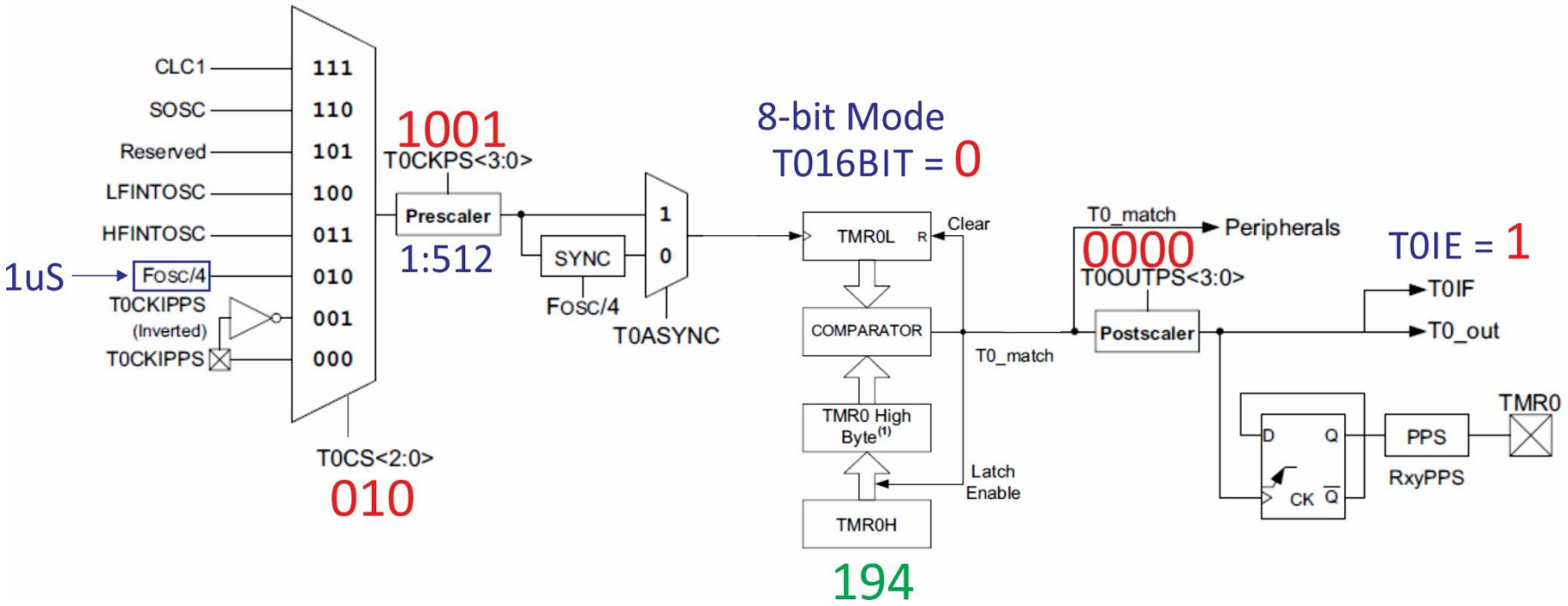
bit 3-1 **Unimplemented:** Read as '0'

bit 0 **INTF:** INT External Interrupt Flag bit(1)
- 1 = The INT external interrupt occurred (must be cleared in software)
- 0 = The INT external interrupt did not occur

Note 1: The External Interrupt GPIO pin is selected by INTPPS (Register 12-1).

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

TMR0: Interrupt every 100mS



Fosc/4 = 1MHz = 1us tick

1us * 512 * (194+1) = 99.84ms

Inline Assembly

```
#asm                    // Start of assembly code
        nop
#endasm                 // End assembly code

//OR
asm("nop");
```

Library Macros

```
NOP();                  // #asm nop #endasm
_delay(t);              // t = processor cycles
__delay_us(t);          // be sure to #define _XTAL_FREQ
CLRWDT();               // #asm clrwt #endasm
```