Analog to Digital Conversion and Pulse Width Modulation

ECE Senior Design
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Analog to Digital Conversion

\[ L_{SB} = \frac{F_{SV}}{2^n} \]

10-bit Conversion and \( V_{\text{ref}} = 5V \)

\[ L_{SB} = \frac{5}{2^{10}} = \frac{5}{1024} = 4.9mV/\text{bit} \]
PIC 16F18324 A/D Converter

- 10-bit Converter
- 11 External Channels Available
- External $V_{REF+}$ and $V_{REF-}$ Available
- Auto Conversion Trigger
10-bit A/D Result Format

For (ADFM = 0):
- MSB
  - bit 7
- 10-bit ADC Result

For (ADFM = 1):
- Unimplemented: Read as '0'
  - bit 7
- MSB
  - bit 7
- 10-bit ADC Result

For ADRESH:
- MSB
  - bit 7
- bit 0

For ADRESL:
- LSB
  - bit 7
- bit 0

Unimplemented: Read as '0'
ADC Clock Selection

TABLE 21-1: ADC CLOCK PERIOD (TAD) VS. DEVICE OPERATING FREQUENCIES

<table>
<thead>
<tr>
<th>ADC Clock Period (TAD)</th>
<th>32 MHz</th>
<th>20 MHz</th>
<th>16 MHz</th>
<th>8 MHz</th>
<th>4 MHz</th>
<th>1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC Clock Source</td>
<td>ADCS&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fosc/2</td>
<td>000</td>
<td>62.5 ns(2)</td>
<td>100 ns(2)</td>
<td>125 ns(2)</td>
<td>250 ns(2)</td>
<td>500 ns(2)</td>
</tr>
<tr>
<td>Fosc/4</td>
<td>100</td>
<td>125 ns(2)</td>
<td>200 ns(2)</td>
<td>250 ns(2)</td>
<td>500 ns(2)</td>
<td>1.0 μs</td>
</tr>
<tr>
<td>Fosc/8</td>
<td>001</td>
<td>0.5 μs(2)</td>
<td>400 ns(2)</td>
<td>0.5 μs(2)</td>
<td>1.0 μs</td>
<td>2.0 μs</td>
</tr>
<tr>
<td>Fosc/16</td>
<td>101</td>
<td>800 ns</td>
<td>800 ns</td>
<td>1.0 μs</td>
<td>2.0 μs</td>
<td>4.0 μs</td>
</tr>
<tr>
<td>Fosc/32</td>
<td>010</td>
<td>2.0 μs</td>
<td>1.6 μs</td>
<td>2.0 μs</td>
<td>4.0 μs</td>
<td>8.0 μs(3)</td>
</tr>
<tr>
<td>Fosc/64</td>
<td>110</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
</tr>
<tr>
<td>ADCRC</td>
<td>x11</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
<td>1.0-6.0 μs(1,4)</td>
</tr>
</tbody>
</table>

Legend: Shaded cells are outside of recommended range.

Note 1: See $T_{AD}$ parameter for ADCRC source typical $T_{AD}$ value.
       2: These values violate the required $T_{AD}$ time.
       3: Outside the recommended $T_{AD}$ time.
       4: The ADC clock period ($T_{AD}$) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock Fosc. However, the ADCRC oscillator source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 21-2: ANALOG-TO-DIGITAL CONVERSION $T_{AD}$ CYCLES

On the following cycle:
- ADRESH:ADRESL is loaded.
- GO bit is cleared,
- ADIF bit is set,
- holding capacitor is reconnected to analog input.

5μS

Enable ADC (ADON bit) and
Select channel (ACS bits)

Set GO bit

Holding capacitor disconnected from analog input (THCD).

Conversion Starts
## ANSELA: PORTA Analog Select

### REGISTER 11-4: ANSELA: PORTA ANALOG SELECT REGISTER

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value at POR and BOR/Value at all other Resets</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td></td>
<td>-n/n</td>
</tr>
<tr>
<td>U-0</td>
<td></td>
<td>-n/n</td>
</tr>
<tr>
<td>R/W-1/1</td>
<td></td>
<td>ANSA5</td>
</tr>
<tr>
<td>R/W-1/1</td>
<td></td>
<td>ANSA4</td>
</tr>
<tr>
<td>U-0</td>
<td></td>
<td>ANSA2</td>
</tr>
<tr>
<td>R/W-1/1</td>
<td></td>
<td>ANSA1</td>
</tr>
<tr>
<td>R/W-1/1</td>
<td></td>
<td>ANSA0</td>
</tr>
</tbody>
</table>

#### Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **-n/n** = Value at POR and BOR/Value at all other Resets

- **‘1’** = Bit is set
- **‘0’** = Bit is cleared

#### Bit Descriptions:

- **Bit 7-6**
  - **Unimplemented:** Read as ‘0’

- **Bit 5-4**
  - **ANSA<5:4>:** Analog Select between Analog or Digital Function on pins RA<5:4>, respectively
  - **1** = Analog input. Pin is assigned as analog input\(^{(1)}\). Digital input buffer disabled.
  - **0** = Digital I/O. Pin is assigned to port or digital special function.

- **Bit 3**
  - **Unimplemented:** Read as ‘0’

- **Bit 2-0**
  - **ANSA<2:0>:** Analog Select between Analog or Digital Function on pins RA<2:0>, respectively
  - **1** = Analog input. Pin is assigned as analog input\(^{(1)}\). Digital input buffer disabled.
  - **0** = Digital I/O. Pin is assigned to port or digital special function.

#### Note 1:

When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.
bit 7-2  

CHS<5:0>: Analog Channel Select bits

111111 = FVR (Fixed Voltage Reference)(2)
111110 = DAC1 output(1)
111101 = Temperature Indicator(3)
111100 = AVss (Analog Ground)
111011 = Reserved. No channel connected.
  
010101 = ANC5(4)
010100 = ANC4(4)
010011 = ANC3(4)
010010 = ANC2(4)
010001 = ANC1(4)
010000 = ANC0(4)
001111 = Reserved. No channel connected.
  
000111 = ANA5
000100 = ANA4
000011 = Reserved. No channel connected.
000010 = ANA2
000001 = ANA1
000000 = ANA0

bit 1  

GO/DONE: ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
   This bit is automatically cleared by hardware when the ADC conversion has completed.
0 = ADC conversion completed/not in progress

bit 0  

ADON: ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current
<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
<th>R/W-0/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADCM</td>
<td>ADCS&lt;2:0&gt;</td>
<td>—</td>
<td>ADNREF</td>
<td>ADPREF&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **u** = Bit is unchanged
- **x** = Bit is unknown
- **n/h** = Value at POR and BOR/Value at all other Resets
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared

**bit 7**

**ADFM**: ADC Result Format Select bit
- 1 = Right justified. Six Most Significant bits of ADRESH are set to ‘0’ when the conversion result is loaded.
- 0 = Left justified. Six Least Significant bits of ADRESL are set to ‘0’ when the conversion result is loaded.

**bit 6-4**

**ADCS<2:0>:** ADC Conversion Clock Select bits
- 111 = ADCRC (dedicated RC oscillator)
- 110 = Fosc/64
- 101 = Fosc/16
- 100 = Fosc/4
- 011 = ADCRC (dedicated RC oscillator)
- 010 = Fosc/32
- 001 = Fosc/8
- 000 = Fosc/2

**bit 3**

**Unimplemented**: Read as ‘0’

**bit 2**

**ADNREF**: V/D Negative Voltage Reference Configuration bit
- When ADON = 0, all multiplexer inputs are disconnected.
- 0 = VREF- is connected to AVSS
- 1 = VREF- is connected to external VREF-

**bit 1-0**

**ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits
- 11 = VREF+ is connected to internal Fixed Voltage Reference (FVR) module<sup>(1)</sup>
- 10 = VREF+ is connected to external VREF+ pin<sup>(1)</sup>
- 01 = Reserved
- 00 = VREF+ is connected to VDD
PWM

Pulse Width Modulation
Amplifier Power Stages
Low Side Drive

[Diagram showing a circuit with labels for Read LATx, TRISx, Data Register, Write LATx, Write PORTx, Data Bus, Read PORTx, To digital peripherals, To analog peripherals, ANSELx, VDD, I/O pin, VSS, LOAD, V+, and ground connections.]
Mosfet $V_{GS}$

Transfer Characteristics

$T_C = 125^\circ C$

$25^\circ C$

$-55^\circ C$

$I_D$ - Drain Current (A)

$V_{GS}$ - Gate-to-Source Voltage (V)
Mosfet $r_{DS(\text{on})}$

On-Resistance vs. Gate-to-Source Voltage

$I_D = 10\text{ A}$

$V_{GS}$ - Gate-to-Source Voltage (V)
H-Bridge Driver

![Diagram of H-Bridge Driver](image-url)
PWM 50% Duty Cycle

Effective Voltage

Voltage = Vdd * 0.50
PWM 20% Duty Cycle

Voltage = Vdd * 0.20

Effective Voltage

20% Duty Cycle
Voltage = Vdd * 0.20
PWM 80% Duty Cycle

Voltage = Vdd * 0.80
PWM Sine Generation

![Graph showing PWM sine generation with voltage and time axes.]

- Voltage axis ranges from 0 to 1.0
- Time axis ranges from 0 to 12000
- The graph illustrates the PWM sine wave with a dashed line and bars representing the PWM signal.
<table>
<thead>
<tr>
<th>Peripheral</th>
<th>PIC16LF8333</th>
<th>PIC16LF8323</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog-to-Digital Converter (ADC)</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Temperature Indicator</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Digital-to-Analog Converter (DAC)</td>
<td>DAC1</td>
<td>●</td>
</tr>
<tr>
<td>Fixed Voltage Reference (FVR)</td>
<td>ADCFVR</td>
<td>●</td>
</tr>
<tr>
<td>CDAFVR</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Digital Signal Modulator (DSM)</td>
<td>DSM1</td>
<td>●</td>
</tr>
<tr>
<td>Numerically Controlled Oscillator (NCO)</td>
<td>NCO1</td>
<td>●</td>
</tr>
<tr>
<td>Capture/Compare/PWM (CCP/ECCP) Modules</td>
<td>CCP1</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>CCP2</td>
<td>●</td>
</tr>
<tr>
<td>Comparators</td>
<td>C1</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>C2</td>
<td>●</td>
</tr>
<tr>
<td>Complementary Waveform Generator (CWG)</td>
<td>CWG1</td>
<td>●</td>
</tr>
<tr>
<td>Configurable Logic Cell (CLC)</td>
<td>CLC1</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>CLC2</td>
<td>●</td>
</tr>
<tr>
<td>Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)</td>
<td>EUSART1</td>
<td>●</td>
</tr>
<tr>
<td>Master Synchronous Serial Port (MSSP)</td>
<td>MSSP1</td>
<td>●</td>
</tr>
<tr>
<td>Pulse-Width Modulator (PWM)</td>
<td>PWM5</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>PWM6</td>
<td>●</td>
</tr>
<tr>
<td>Timers</td>
<td>Timer0</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>Timer1</td>
<td>●</td>
</tr>
<tr>
<td>•</td>
<td>Timer2</td>
<td>●</td>
</tr>
</tbody>
</table>

**CCP & PWM**

- 2 CCP Modules
- 2 PWM Modules
- Timer 2 Sets Freq
Dedicated PWM Module

PWM Output on PPS

Registers:
- TMR2
- PR2
- PWMxCON
- PWMxDCH
- PWMxDCL
REGISTER 18-1: PWMxCON: PWM CONTROL REGISTER

<table>
<thead>
<tr>
<th>R/W-0/0</th>
<th>U-0</th>
<th>R-0</th>
<th>R/W-0/0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>PWMxEN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PWMxOUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PWMxPOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

R = Readable bit       W = Writable bit       U = Unimplemented bit, read as ‘0’
u = Bit is unchanged    x = Bit is unknown     -n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set        ‘0’ = Bit is cleared

bit 7  PWMxEN: PWM Module Enable bit
       1 = PWM module is enabled
       0 = PWM module is disabled

bit 6  Unimplemented: Read as ‘0’

bit 5  PWMxOUT: PWM module output level when bit is read.

bit 4  PWMxPOL: PWMx Output Polarity Select bit
       1 = PWM output is active-low
       0 = PWM output is active-high

bit 3-0 Unimplemented: Read as ‘0’
Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ’0’
- u = Bit is unchanged
- x = Bit is unknown
- -n/n = Value at POR and BOR/Value at all other Resets
- ’1’ = Bit is set
- ’0’ = Bit is cleared

bit 7
Unimplemented: Read as ’0’

bit 6-3
T2OUTPS<3:0>: Timer2 Output Postscaler Select bits
1111 = 1:16 Postscaler
1110 = 1:15 Postscaler
1101 = 1:14 Postscaler
1100 = 1:13 Postscaler
1011 = 1:12 Postscaler
1010 = 1:11 Postscaler
1001 = 1:10 Postscaler
1000 = 1:9 Postscaler
0111 = 1:8 Postscaler
0110 = 1:7 Postscaler
0101 = 1:6 Postscaler
0100 = 1:5 Postscaler
0011 = 1:4 Postscaler
0010 = 1:3 Postscaler
0001 = 1:2 Postscaler
0000 = 1:1 Postscaler

bit 2
TMR2ON: Timer2 On bit
1 = Timer2 is on
0 = Timer2 is off

bit 1-0
T2CKPS<1:0>: Timer2 Clock Prescale Select bits
11 = Prescaler is 64
10 = Prescaler is 16
01 = Prescaler is 4
00 = Prescaler is 1

Sets Flag bit TMR2IF
Peripheral Pin Select

Inputs:
Each Peripheral Has A PPS Register
xyzPPS – Specifies the Peripheral

Outputs:
Each I/O Pin Has A PPS Register
RxyPPS – Specifies the Pin
RxyPPS<4:0> Pin Rxy Output Source Selection bits

Legend:
- **R**: Readable bit
- **W**: Writable bit
- **U**: Unimplemented bit, read as ‘0’
- **u**: Bit is unchanged
- **x**: Bit is unknown
- **-n/n**: Value at POR and BOR/Value at all other Resets
- **‘1’**: Bit is set
- **‘0’**: Bit is cleared

Unimplemented: Read as ‘0’

bit 7-5

Bit 4-0

- **11111**: Rxy source is DSM
- **11110**: Rxy source is CLKR
- **11101**: Rxy source is NCO
- **11100**: Rxy source is TMR0
- **11011**: Reserved
- **11010**: Reserved
- **11001**: Rxy source is SDO/SDA\(^{(1)}\)
- **11000**: Rxy source is SCK/SCI\(^{(1)}\)
- **10111**: Rxy source is C2OUT\(^{(2)}\)
- **10110**: Rxy source is C1OUT
- **10101**: Rxy source is DT\(^{(1)}\)
- **10100**: Rxy source is TX/CK\(^{(1)}\)
- **01111**: Rxy source is CCP2
- **01110**: Rxy source is CCP1
- **01101**: Rxy source is CWG1D\(^{(1)}\)
- **01100**: Rxy source is CWG1C\(^{(1)}\)
- **01001**: Rxy source is CWG1B\(^{(1)}\)
- **01000**: Rxy source is CWG1A\(^{(1)}\)
- **...**
- **00111**: Reserved
- **00110**: Reserved
- **00101**: Rxy source is CLC2OUT
- **00100**: Rxy source is CLC1OUT
- **00011**: Rxy source is PWM6
- **00010**: Rxy source is PWM5
- **00001**: Reserved
- **00000**: Rxy source is LATxv